Alan Stern, Rowland Institute at Harvard
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Kangrejos, Copenhagen, Denmark, September 8, 2024

Lifetime-End Pointer Zap & How to Avoid OOTA Without Really Trying

Overview

This is just an overview, not a replacement for the papers themselves

- P2414R10 “Pointer lifetime-end zap proposed solutions”
  - https://www.open-std.org/jtc1/sc22/wg21/docs/papers/2025/p2414r10.pdf
- P3347R5 Invalid/Prospective Pointer Operations
  - https://www.open-std.org/jtc1/sc22/wg21/docs/papers/2025/p3347r5.pdf
  - Based on Davis Herring’s P2434R4 “Nondeterministic pointer provenance”
    - https://www.open-std.org/jtc1/sc22/wg21/docs/papers/2025/p2434r4.html
- P3790R1 “Pointer lifetime-end zap proposed solutions: Bag-of-bits pointer class”
  - https://www.open-std.org/jtc1/sc22/wg21/docs/papers/2025/p3790r1.pdf
- P3692R2 “How to Avoid OOTA Without Really Trying”
  - https://www.open-std.org/jtc1/sc22/wg21/docs/papers/2025/p3692r2.pdf

Overview

- Lifetime-end pointer zap
- Out-of-thin-air (OOTA) cycles
- Where are we on OOTA?
- Leverage restrictions:
  - Real computer systems
  - Speculate properly or not at all
  - Existing restrictions for volatile atomics
  - No invention or repurposing of atomic loads
  - Tooling looks at object code
- Future directions

Lifetime-End Pointer Zap

Problem Restatement (C11, 1/2)

```
struct node_t* _Atomic top;

void list_push(value_t v)
{
  struct node_t *newnode = (struct node_t *) malloc(sizeof(*newnode));
  Struct node_t *next = atomic_load(&top);

  set_value(newnode, v);
  do {
    set_next(newnode, next);
    // newnode’s next pointer may have become invalid
  } while (!atomic_compare_exchange_weak(&top, &next, newnode));
}
```

Problem Restatement (C11, 2/2)

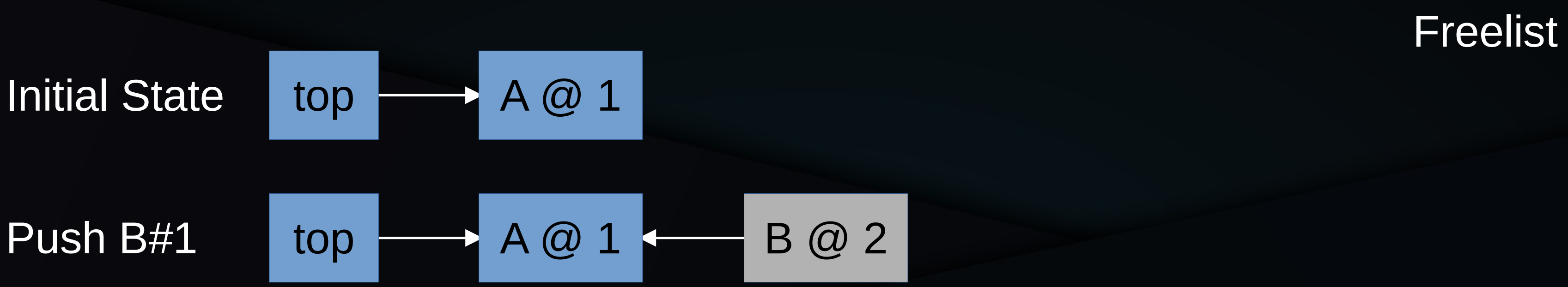
```
void list_pop_all()
{
  struct node_t *p = atomic_exchange(&top, NULL);

  while (p) {
    struct node_t *next = p->next;

    foo(p);
    free(p);
    p = next;
  }
}
```

Problem Illustration (C11)

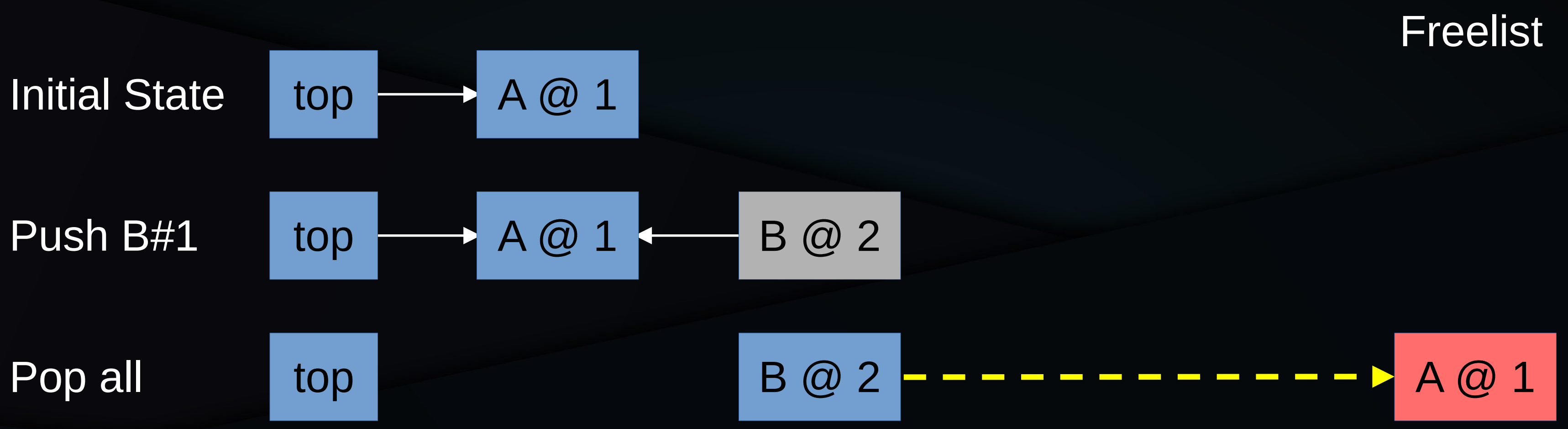
Freelist

Initial State top → A @ 1

Problem Illustration (C11)



Problem Illustration (C11)



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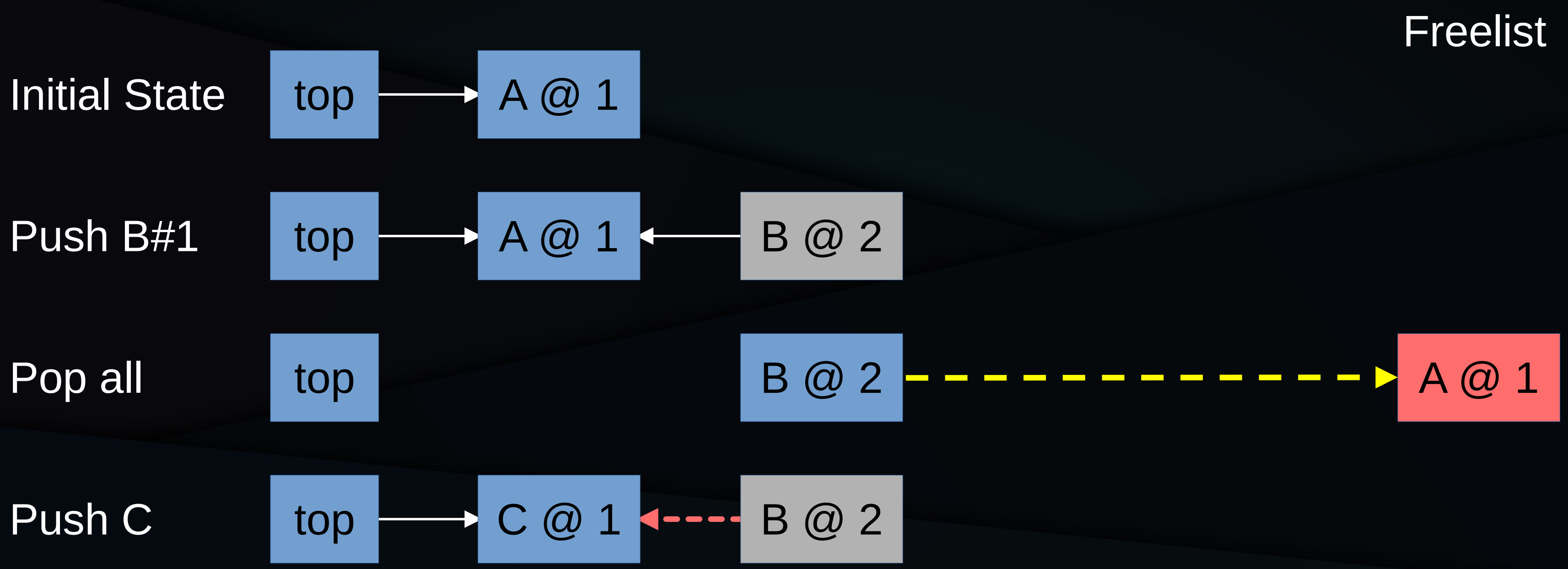

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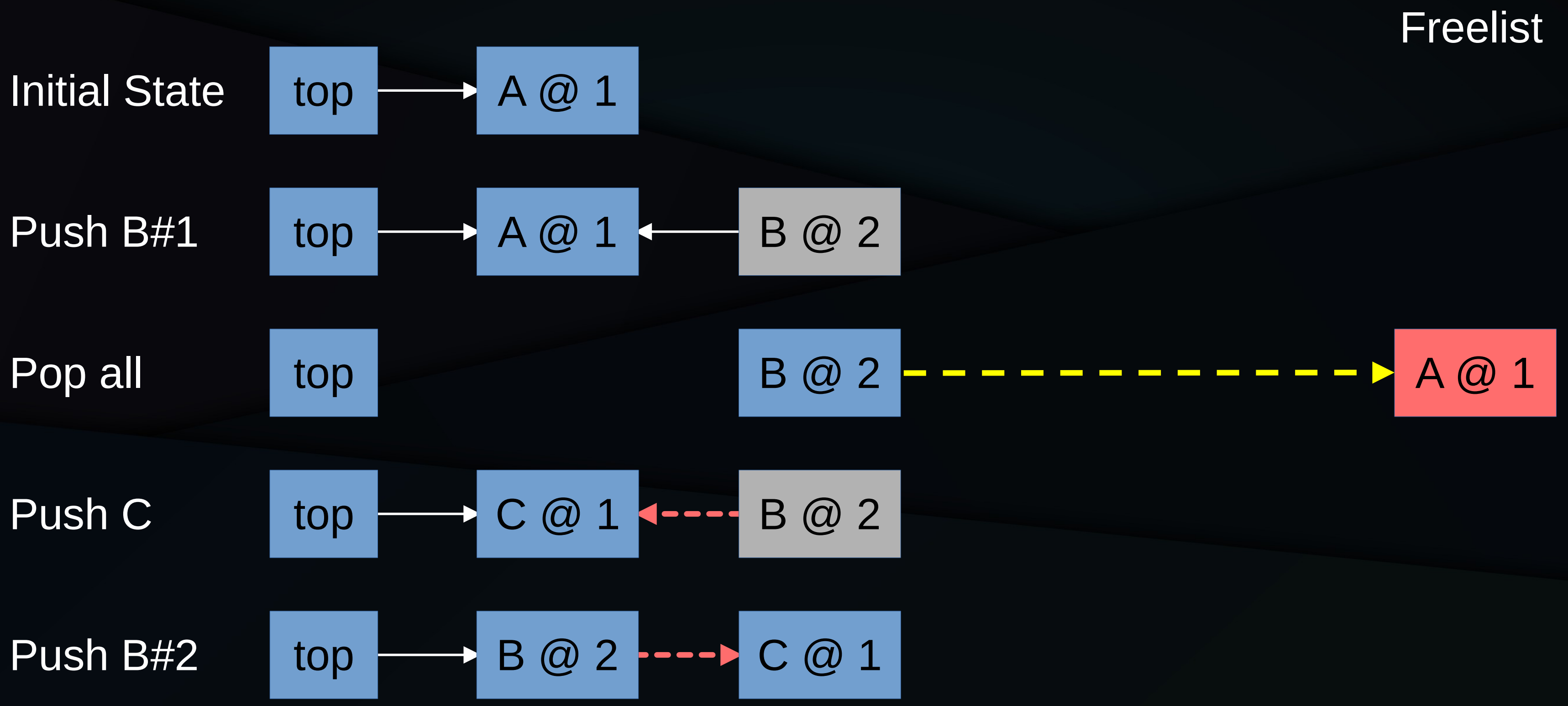

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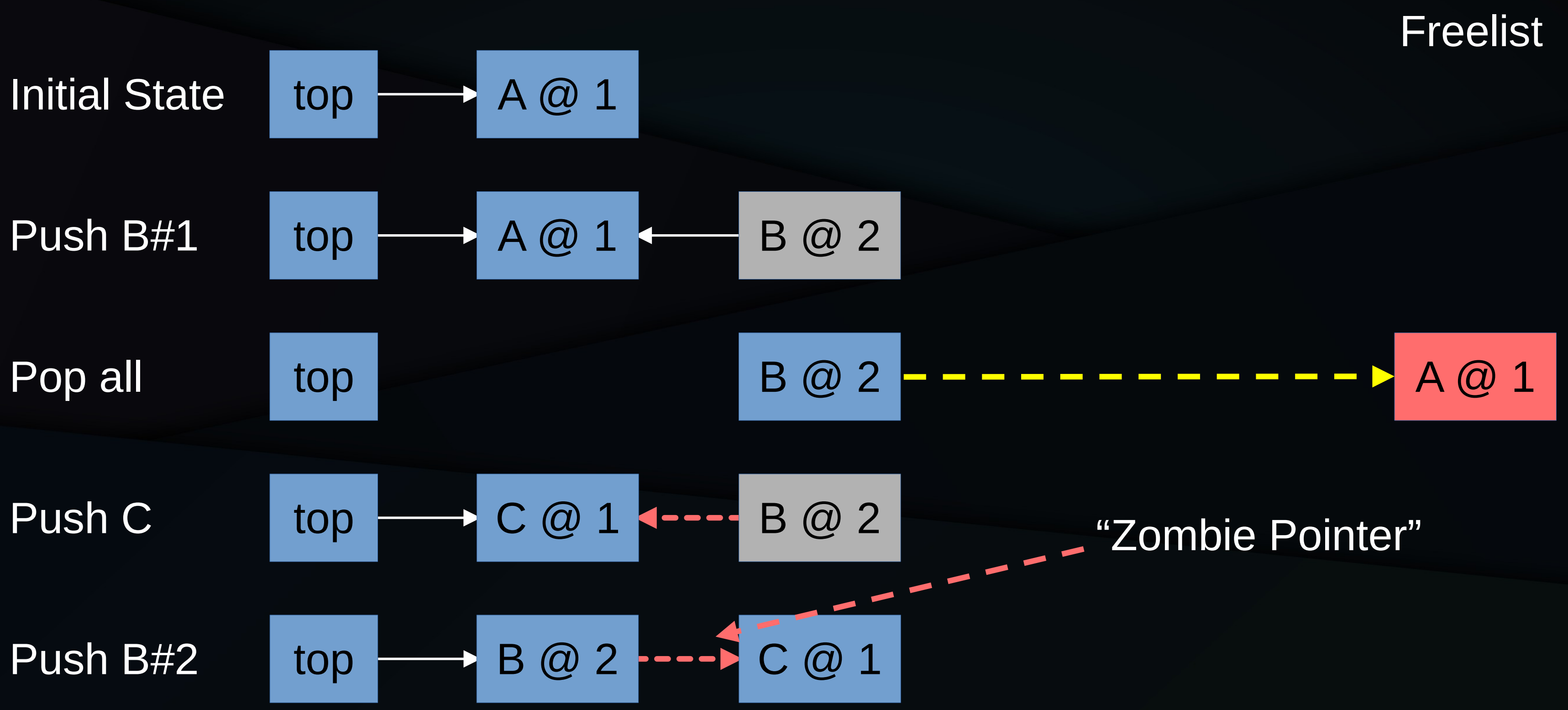

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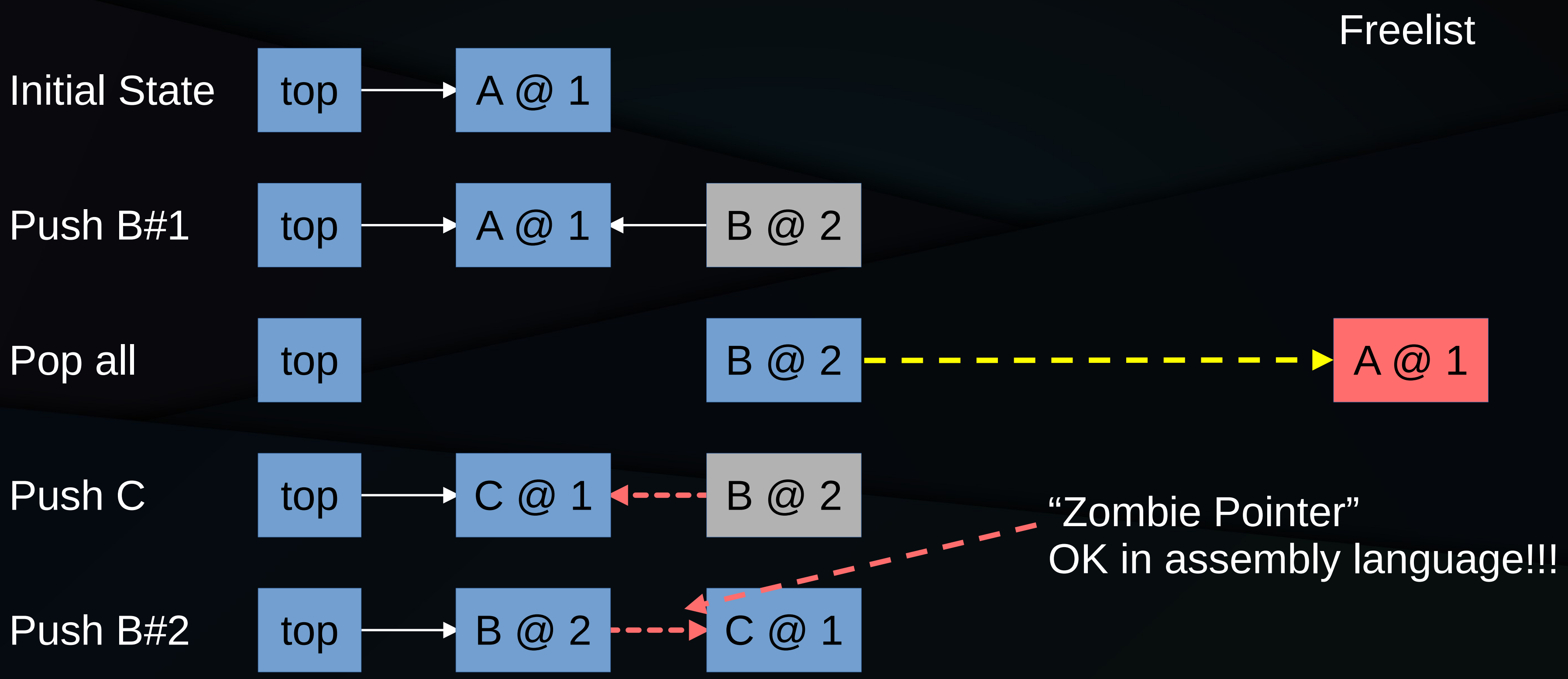

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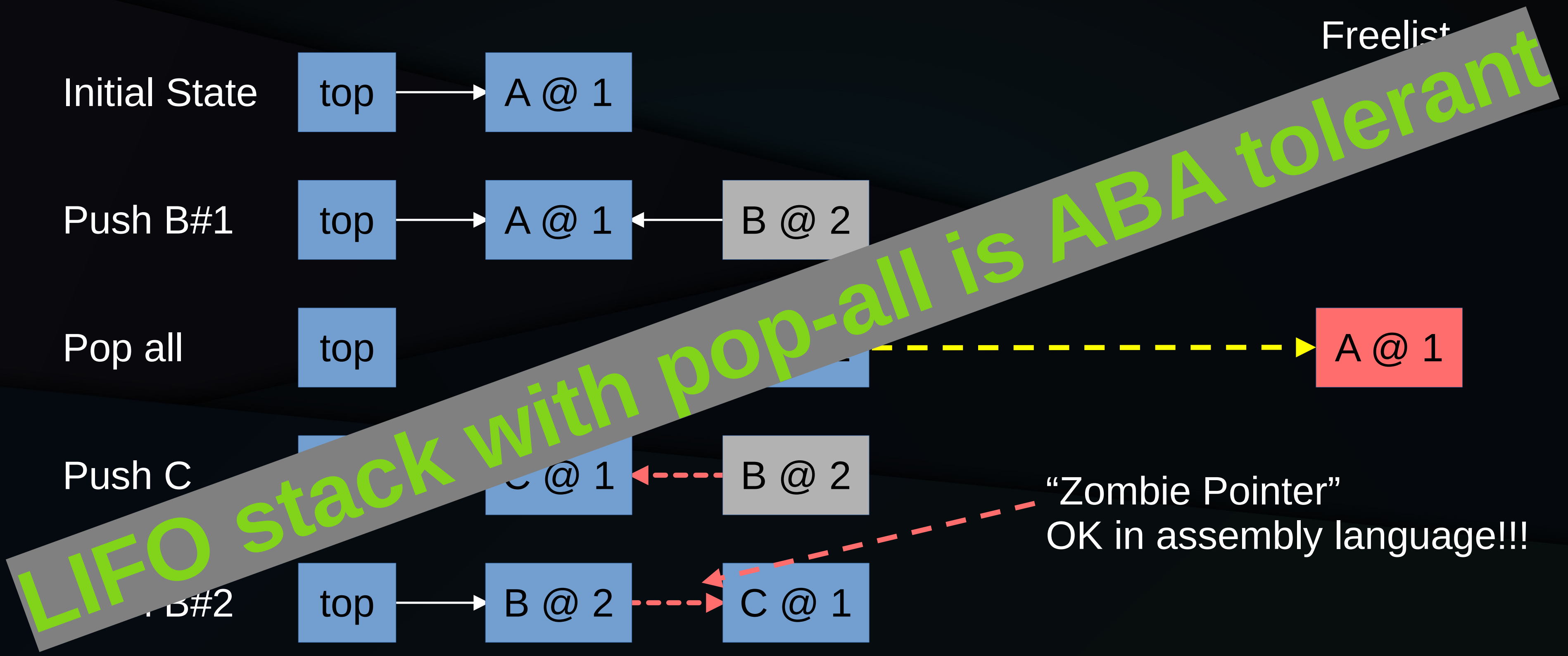

This is Real and Isn’t Going Away

- LIFO stack described by Treiber in 1986
  - Written in IBM BAL, avoiding issues with compilers
- LIFO stack alluded to in early 1970s
- LIFO stack implemented in Rust library
  - Though with `pop()`, not `pop_all()`.
- Used in heavily production in many languages
  - Often open-coded, often inadvertently reinvented

OK, OK, What is New Since 2024???

C and C++: Pointer Provenance

- Pointers contain bits and also “provenance”
  - Compiler may assume that pointers from two different calls to the allocator are unequal
  - Some provenance might be part of pointer value (ARM MTE)
- Provenance may be erased
  - Conversion to integer, I/O, optimization frontiers
- Davis Herring C++ proposal (P2434R4) provides “angelic provenance”, **but now limited**

C++: Angelic Provenance

- Davis Herring P2434R4 (“Nondeterministic pointer provenance”) restricts provenance restoration
  - Conversion from integer, I/O, optimization frontiers
  - At which point, the compiler must choose provenance (if any) that allows the program to be well-formed
    - **But compiler need not consider objects where provenance restoration happens-before the beginning of that object’s storage duration**

C++: Angelic Provenance

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  - Conversion from integer, I/O, optimi[illegible]tiers
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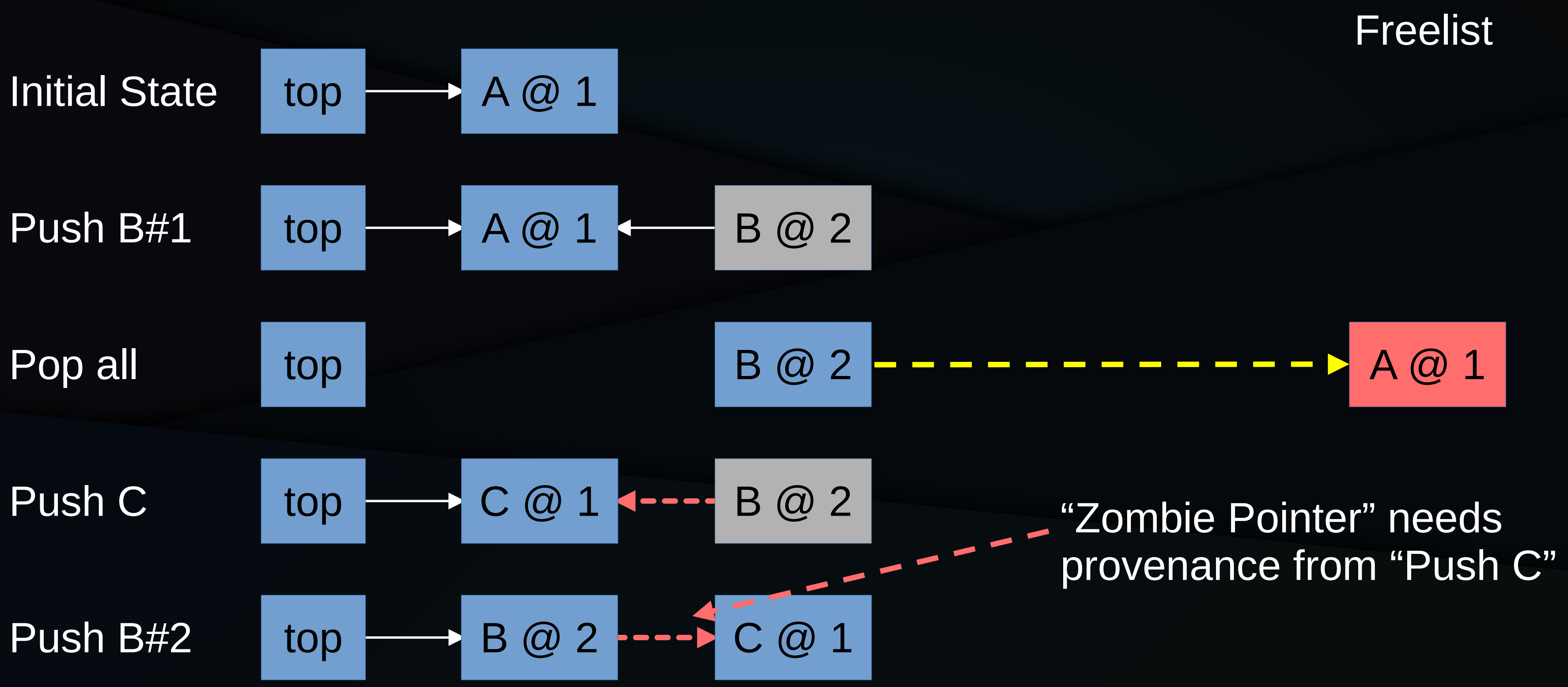
    - **But com[illegible] not consider objects where pr[illegible] restoration happens-before the beginning of that object’s storage duration**

Not enough for LIFO stack…

Problem Illustration (C11)



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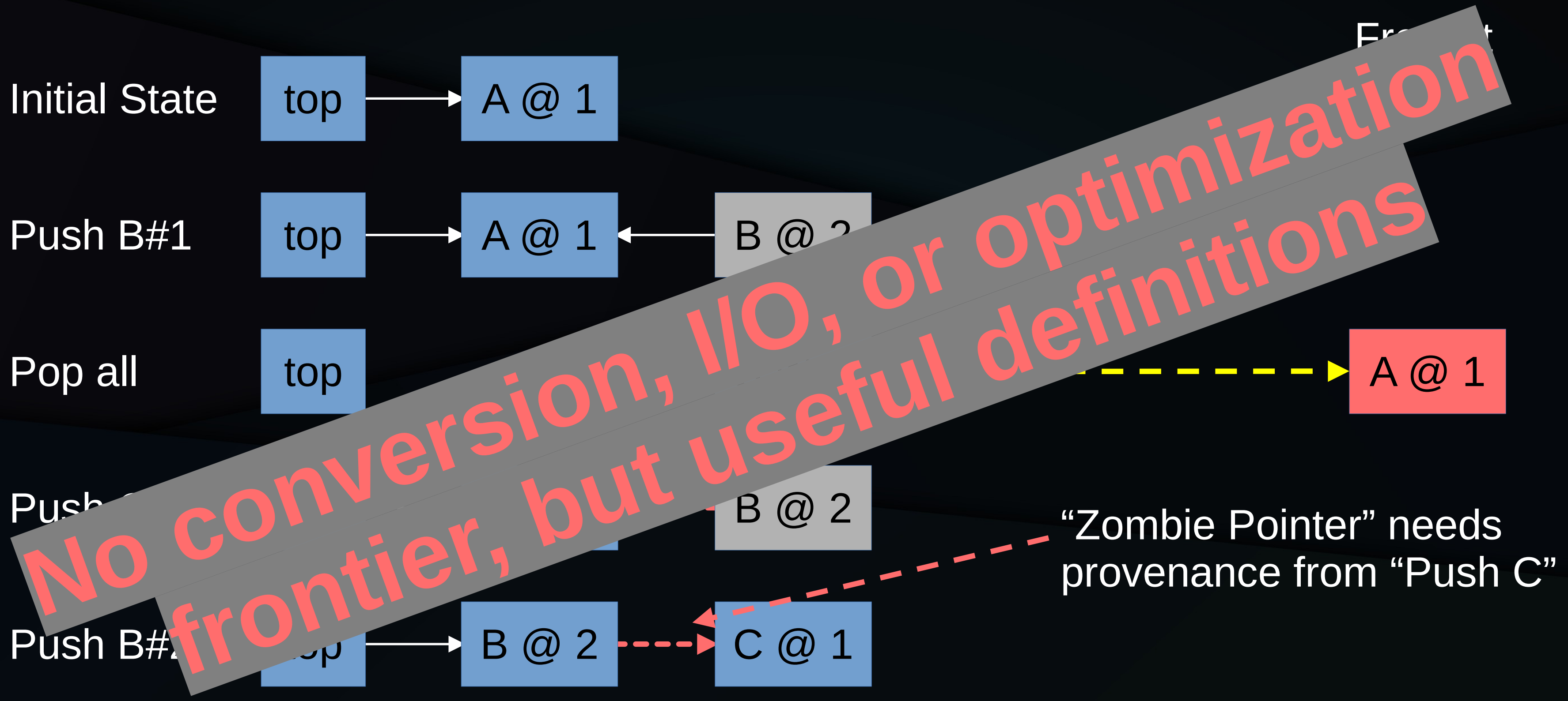

What Else Is Needed?

- P2414R10 (“Pointer lifetime-end zap proposed solutions”): Provenance restoration results from:
  - Conversions to/from atomic<T *>
    - Including old pointer referenced by successful CAS operations
  - Volatile accesses involving pointers
- P3347R5 (“Pointer lifetime-end zap proposed solutions: Tighten IDB for invalid and prospective pointers”)
  - Glvalue-to-rvalue conversions from invalid pointers must produce representation values consistent with those of the lvalue
- P3790R1 (“Pointer lifetime-end zap proposed solutions: bag-of-bits pointer class”): Provenance restoration results from:
  - `ptr_bits<T>` **(But now internal representation not visible to user per IBM System i)**
  - `launder_ptr_bits()` “identity” function

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  - `ptr_bits<T>` **(But now internal representation not visible to user per IBM System i)**
  - `launder_ptr_bits()` “identity” function

Not all that much!!!

Status in C++ Committee

- All progressing through C++ committee:
  - P2414R10 “Pointer lifetime-end zap proposed solutions”
  - P3347R5 “Pointer lifetime-end zap proposed solutions: Tighten IDB for invalid and prospective pointers”
  - P3790R1 “Pointer lifetime-end zap proposed solutions: bag-of-bits pointer class “
  - Davis Herring’s P2434R4 “Nondeterministic pointer provenance”
- No guarantees, but best progress thus far

Pointer-Zap Discussion

OOTA Cycles

Proposed Change to C++ Standard

Proposed Change to C++ Standard

- P3692R2 (“How to Avoid OOTA Without Really Trying”):
  - After N5008 33.5.4p8 ([atomics.order])33.5.4p8 ([atomics.order]):
    - “Implementations should ensure that no “out-of-thin-air” values are computed that circularly depend on their own computation. [Note 6 *… example …*]”
  - Add the following:
    - “Compiler-based implementations whose binaries run on conventional hardware are guaranteed not to compute out-of-thin-air values in programs that are free of undefined behavior, as long as they restrict themselves to thread- at-a-time analysis and and treat non-volatile atomic accesses as if they were volatile, except that, when permitted by the as-if rule, they may omit accesses, merge accesses to the same object, or reorder accesses to different objects.”

Proposed Change to C++ Standard

- P3692R2 ("How to Avoid OOTA Without Really T… "):
  - After N5008 33.5.4p8 ([atomics.order])33.5 … rder]):
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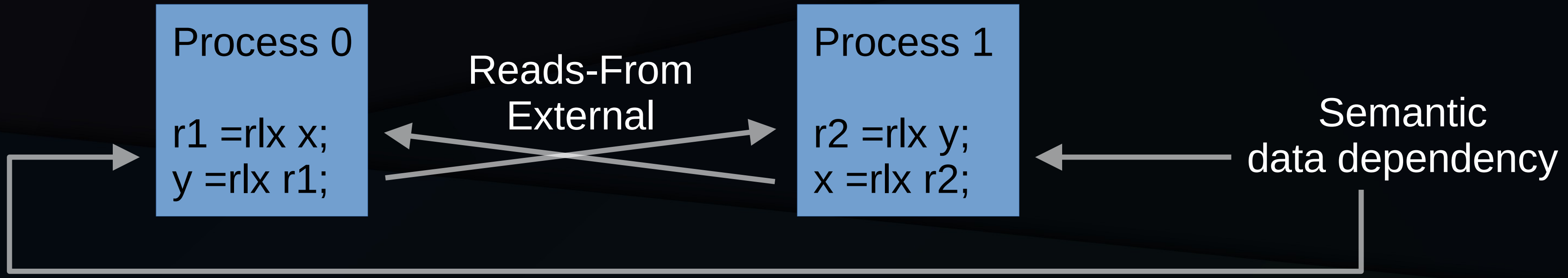
  - Add the following:
    - "Compiler-bas… ies run on conventional hardware are guarante… alues in programs that are free of und… ng as t… estrict themselves to thread- at-a-time analysis an… olatile atomic accesses as if they were volatile, except that, when p… ed by the as-if rule, they may omit accesses, merge accesses to the same object, or reorder accesses to different objects."

Earlier version well-received at June Sofia C++ Standards Committee meeting

OOTA Cycles: Background

OOTA Cycles

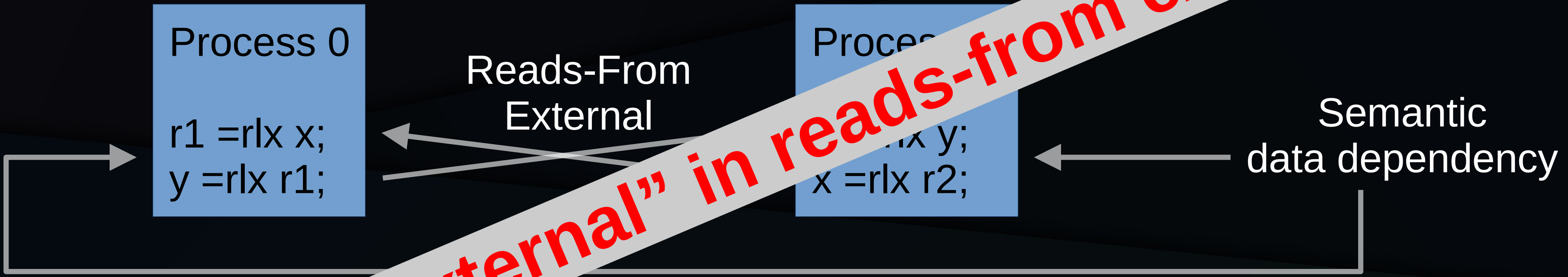
- Self-satisfying load-buffering cycle, x==y==42



Relaxed load or store denoted by “=rlx”

OOTA Cycles

- Self-satisfying load-buffering cycle, x==y==42



Why “external” in reads-from external?

OOTA Cycles: Reads-From Internal

```
r1 =rlx X;
Y =rlx r1;
r2 =rlx Y;
Z =rlx r2;
```

rfi

OOTA Cycles: Reads-From Internal

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r1 =rlx X;
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Z =rlx r2;
```

```
r1 =rlx X;
Z =rlx r1;
Y =rlx r1;
r2 = r1;
```

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r1 =rlx X;
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r1 =rlx X;
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Y =rlx r1;
r2 = r1;
```

Compiler eliminated the read from Y so that
the store to Z can now occur before the store to Y

OOTA Cycles: Reads-From Internal

```
r1 =rlx X;
Y =rlx r1;
r2 =rlx Y;
Z =rlx r2;
```

```
r1 =rlx X;
Z =rlx    ;
Y    lx r1;
r2 = r1;
```

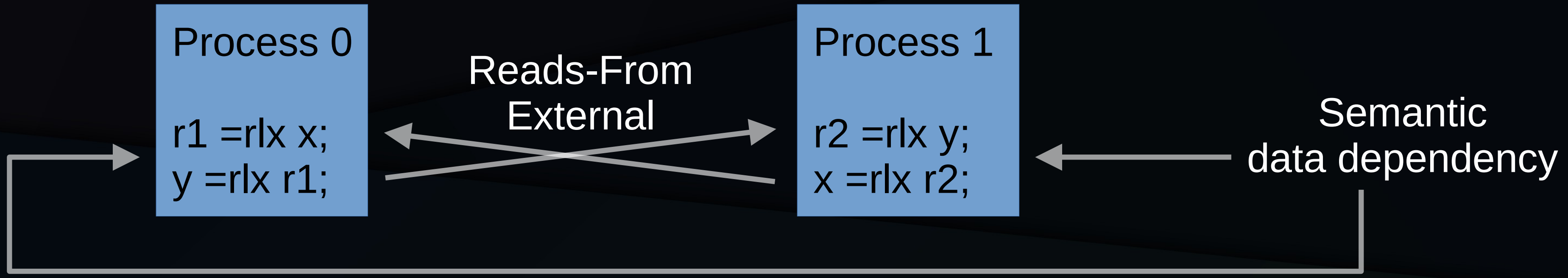
Hence “external” in reads-from external

…piler eliminated the read from Y so that
…e store to Z can now occur before the store to Y

See Section 2.1 (“OOTA: rf vs. rfe”) of P3692R2

OOTA Cycles, Original Diagram

- Self-satisfying load-buffering cycle, x==y==42



OOTA Cycles, Original Diagram

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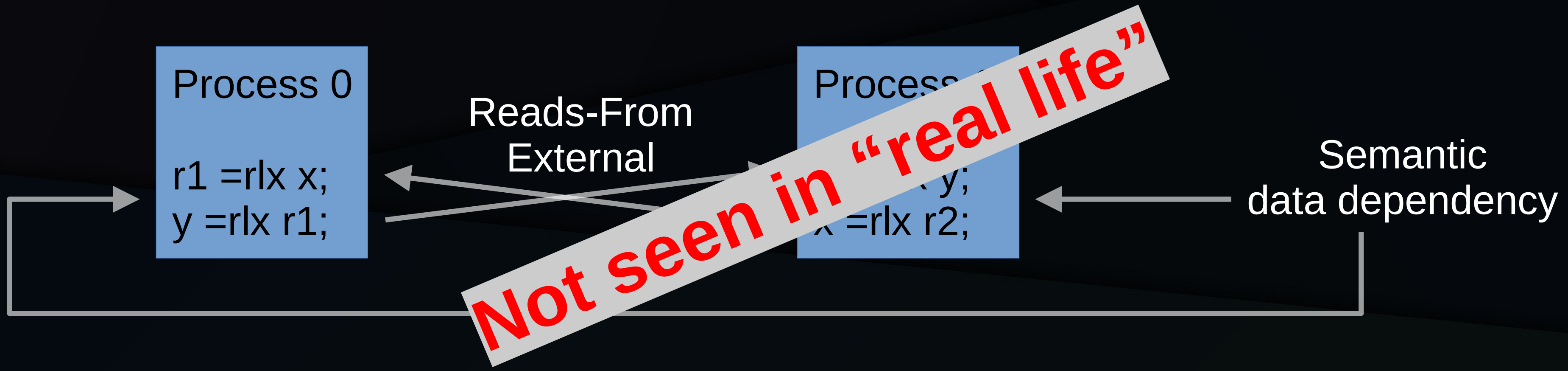

OOTA Cycles, Original Diagram

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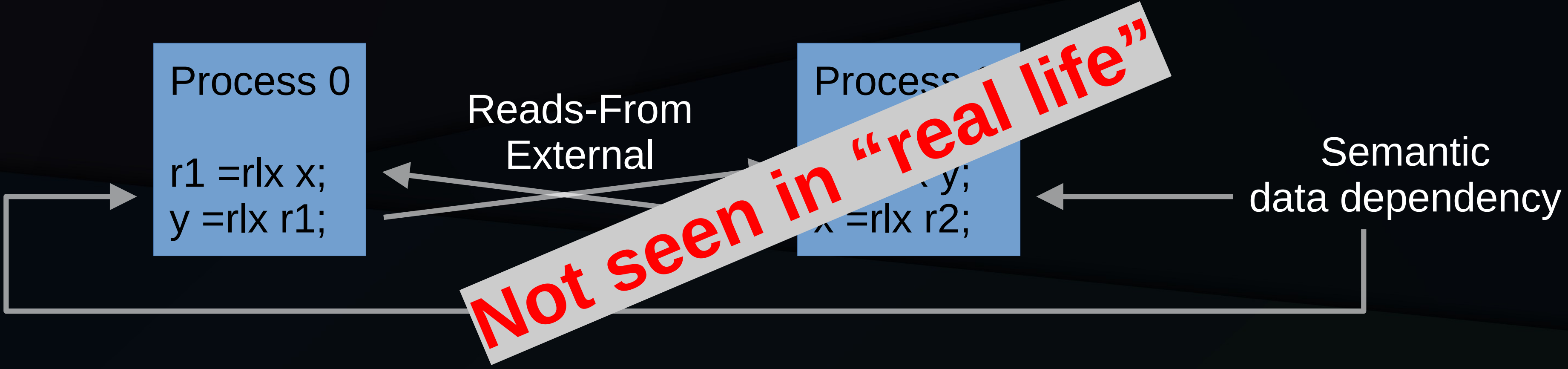
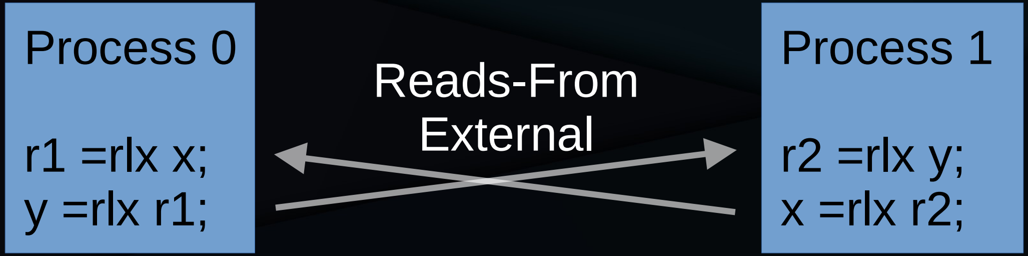


Why???

Where Are We on OOTA?

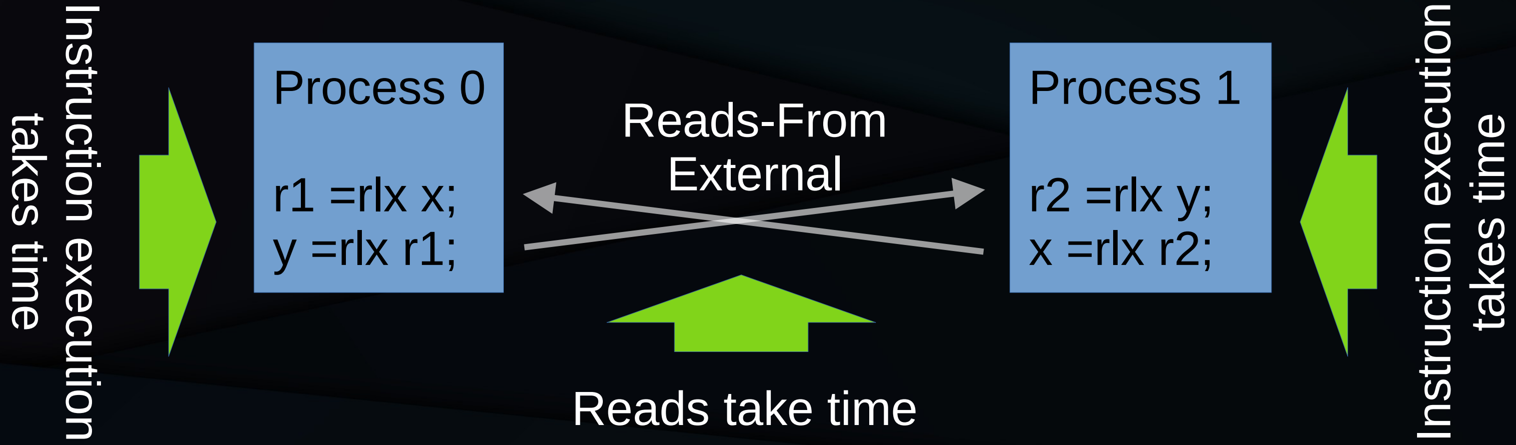
Where Are We on OOTA? (TL;DR)



Where Are We on OOTA? (TL;DR)

Reads take time

Where Are We on OOTA? (TL;DR)



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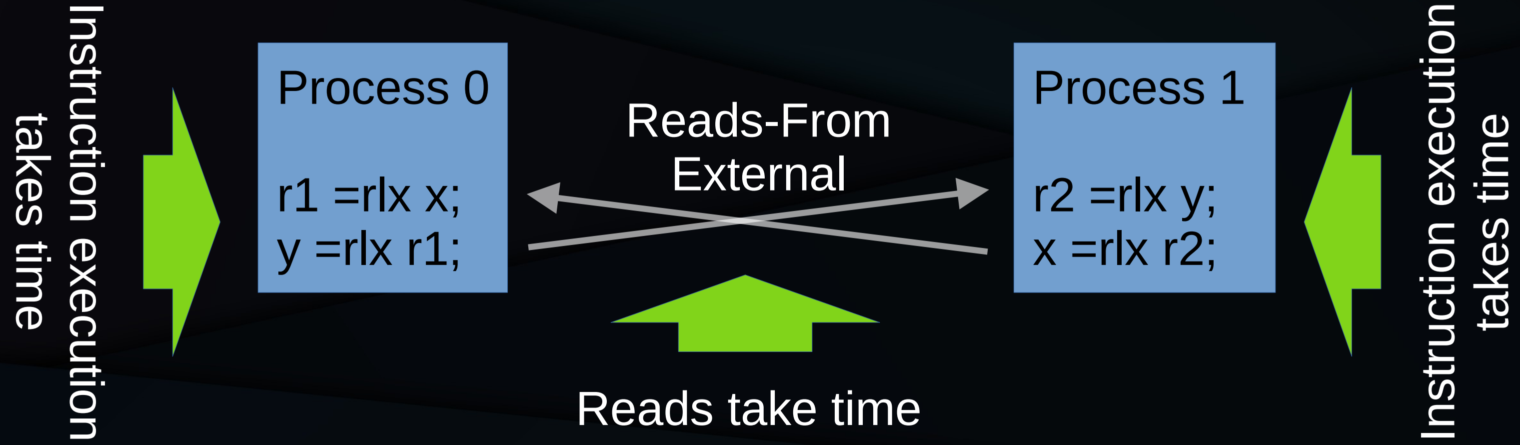
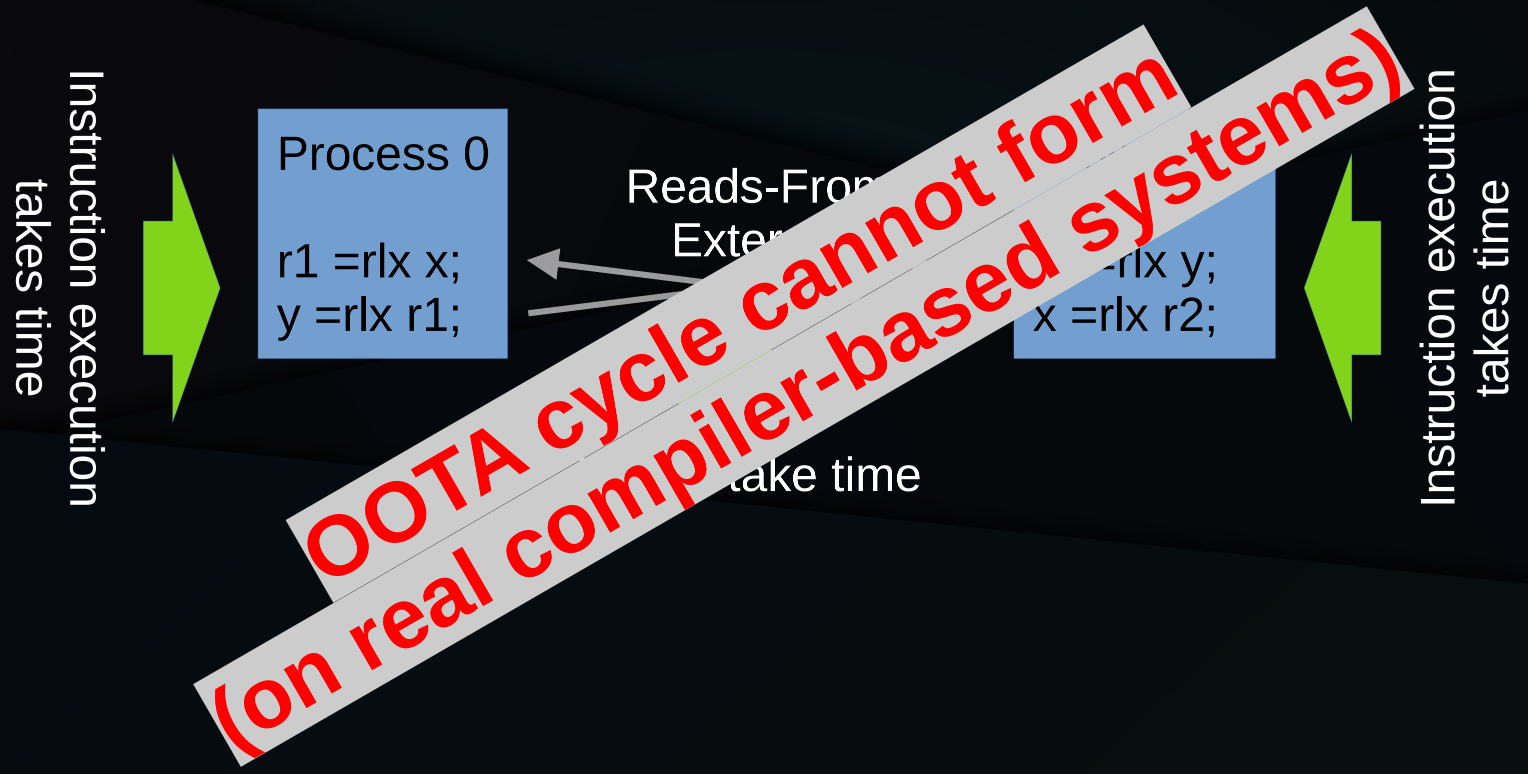


To form an OOTA cycle, at least one step must go backwards in time!!!

Where Are We on OOTA? (TL;DR)



To form an OOTA cycle, at least one step must go backwards in time!!!

Where Are We on OOTA?

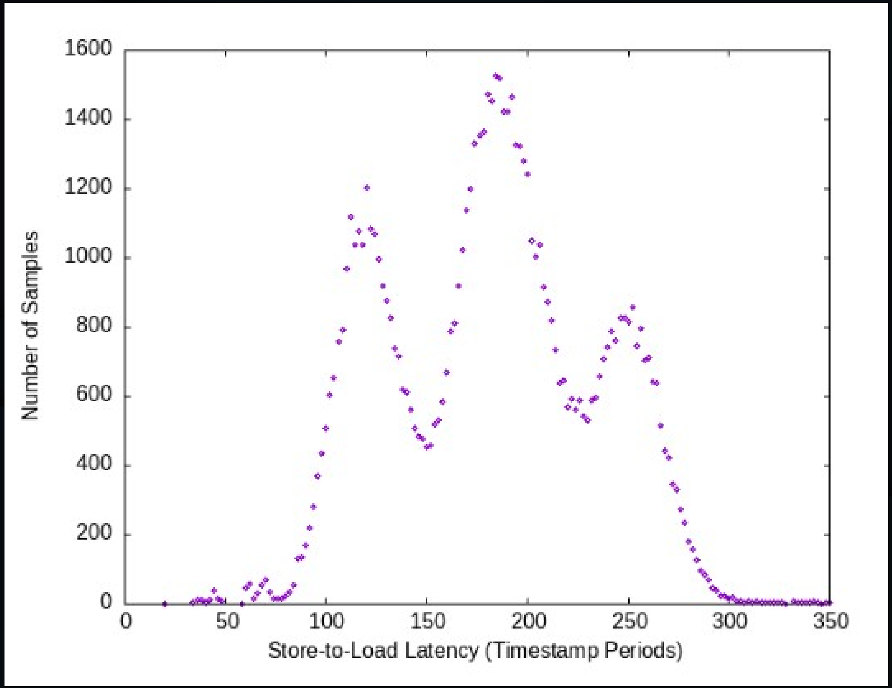
- Generalized “OOTA Cycle” (Section 2.2.2)
- Fundamental property of semantic dependency (Sections 5.3 and 6.1)
- Demonstrate OOTA-freedom under restrictions (Sections 6.2-6.4 for demonstration, 4.4 for restrictions)

Leverage Restrictions

Real Computer Systems

Real Computer Systems: Store-to-Load

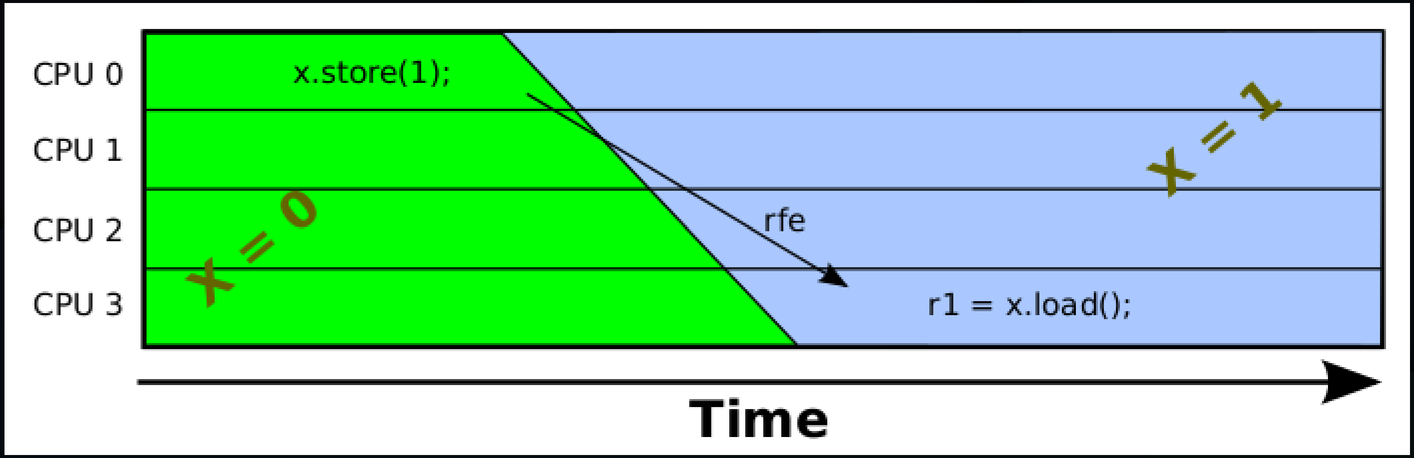
- Store-to-load links are temporal*



* The event that is logically first must happen before the other event in real-world time
Dual-socket Intel(R) Xeon(R) Gold 6138 CPUs @ 2.00 GHz, 80 hardware threads total: Measure beginning of store to end of load

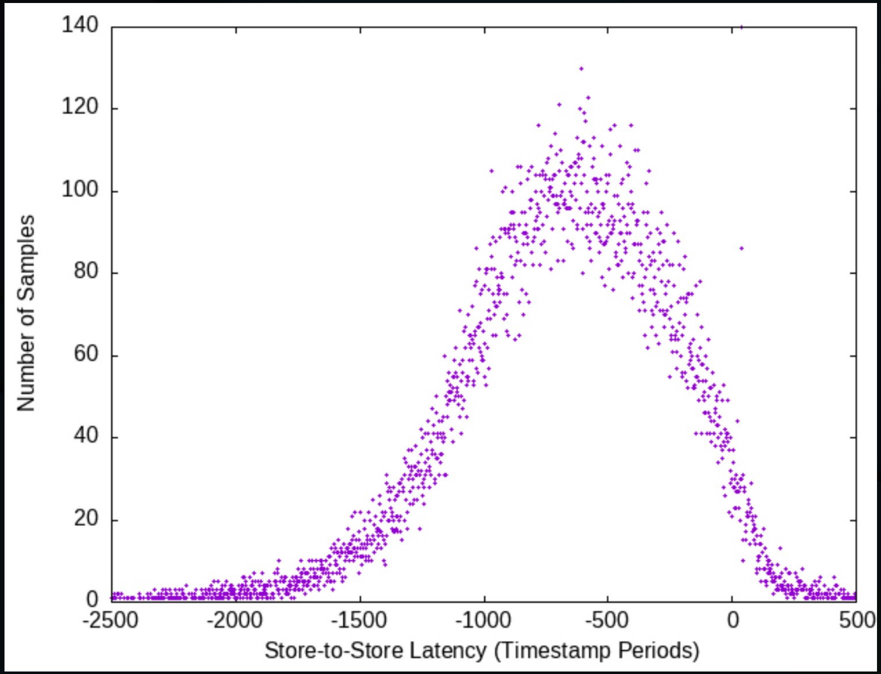
Real Computer Systems: Store-to-Load

- Store-to-load links are temporal: HW view



Real Computer Systems: Store-to-Store

- Store-to-store links are atemporal*



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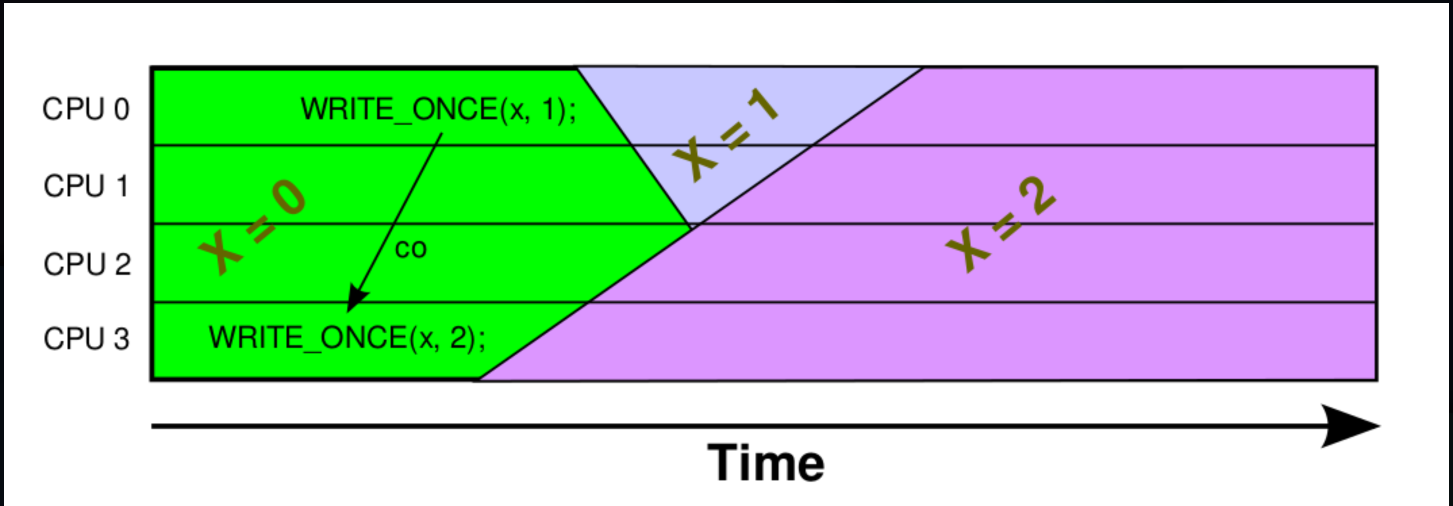
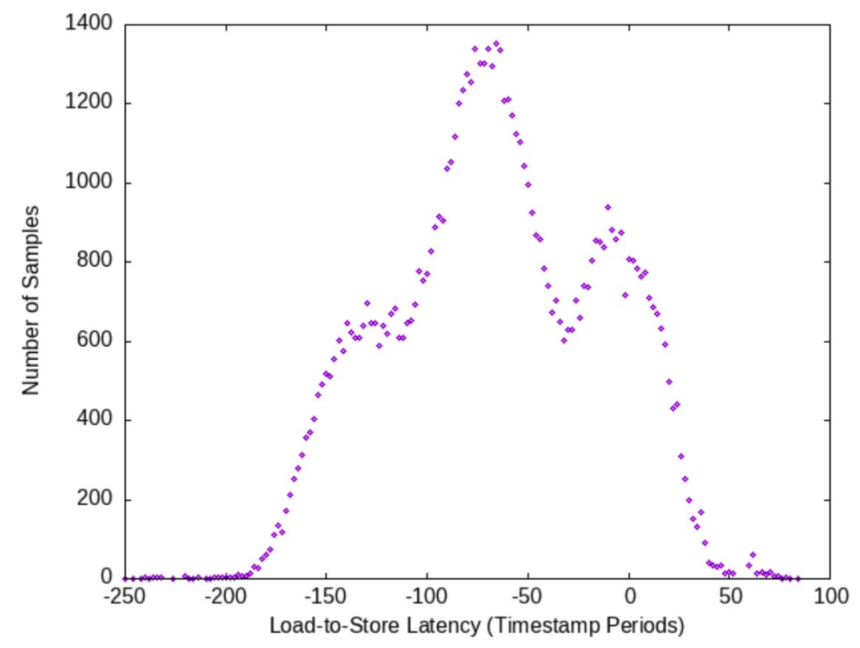


“co” is “modification order” in the C++ memory model

Real Computer Systems: Load-to-Store

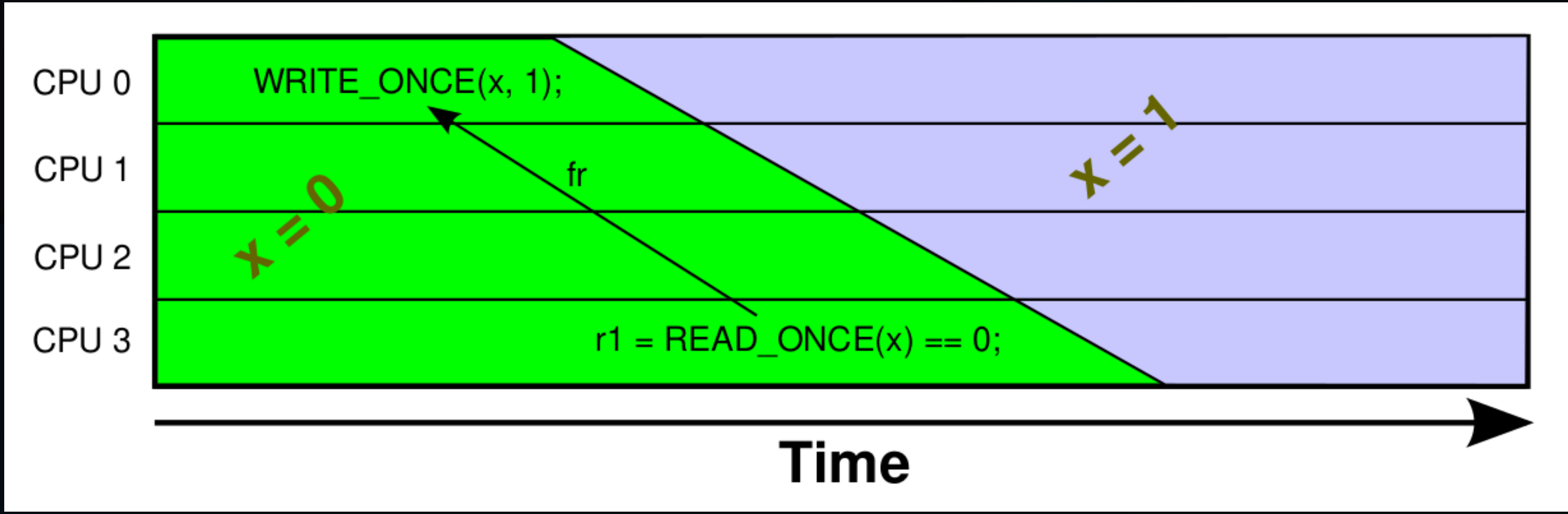
- Load-to-store links are atemporal



Dual-socket Intel(R) Xeon(R) Gold 6138 CPUs @ 2.00 GHz, 80 hardware threads total: Measure beginning of load to end of store

Real Computer Systems: Load-to-Store

- Load-to-store links are atemporal: HW view



“fr” is “from reads”, which connects a read to a write that happened too late to affect the value loaded

Real Computer Systems: Summary

- Load-to-store links: Atemporal
- Store-to-store links: Atemporal
- Store-to-load links: Temporal
  - And thus have ordering properties on the cheap

See Appendix A (“Interthread Communications”) of wg21.link/P3064R2 (“How to Avoid OOTA Without Really Trying”)

Speculate Properly or Not At All

Speculate Properly or Not At All

```
r1 =speculate_x 2;
r2 = somefunc(r1);
Y = r2;
```

atemporal!!!

```
X =rlx 1;
```

Speculate Properly or Not At All

X =rlx 1;

r1 =speculate$_x$ 2;

r2 = somefunc(r1);

X = r2;

Also improper!!!

Don’t just guess! Guess and then check!!!

Speculate Properly or Not At All

```
X =rlx 1;
```

temporal!!!

```
r1 =speculate_x 2;
r2 = somefunc(r1);
```

~~Y = r2;~~

```
r3 =rlx X; // 1, not 2!
if (r1 != r3)
    r2 = somefunc(r3);
Y = r2;
```

Speculate Properly or Not At All

```
X =rlx 1;
```

temporal!!!

```
r1 =speculate_X 2;
r2 = somefun      );
```

~~Y = r2;~~

```
r3              1, not 2!
               r3)
    r2 = somefunc(r3);
Y = r2;
```

Speculation must be checked against the value from an actual load!!!

See Section 1.1 (“Brief OOTA Overview”) and Section 5.2 (“Instruction Ordering”) of P3692R2

Existing Restrictions on Volatile Atomics

Existing Restrictions on Volatile Atomics

- Compiler may not:
  - Reorder accesses
  - Invent, duplicate, or repurpose accesses
  - Merge or fuse accesses
  - Omit accesses
- Relax restrictions for non-volatile atomics?

No Atomic-Load Invention/Repurposing

No Atomic-Load Invention

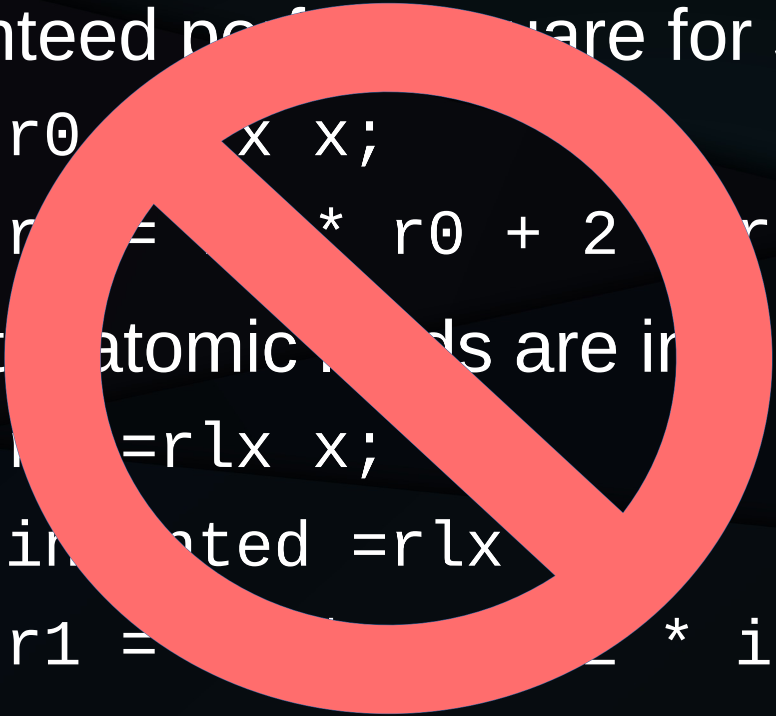
- Guaranteed perfect square for small X:

```
int r0 =rlx x;
int r1 = r0 * r0 + 2 * r0 + 1;
```

- But not if atomic loads are invented!!!

```
int r0 =rlx x;
int invented =rlx x;
int r1 = r0 * r0 + 2 * invented + 1;
```

No Atomic-Load Invention



- Guaranteed pe[illegible]are for small X:

```
int r0 [illegible]x x;
int r[illegible]= [illegible]* r0 + 2 [illegible]r0 + 1;
```

- But not [illegible]atomic [illegible]ds are in[illegible]nted!!!

```
int r[illegible]=rlx x;
int in[illegible]ted =rlx [illegible]
int r1 = [illegible]* invented + 1;
```

No Atomic-Load Repurposing

- Guaranteed perfect square for small X:

```
r2 =rlx x;
do_something(r2); // No synchronization or stores to x
int r0 =rlx x;
int r1 = r0 * r0 + 2 * r0 + 1;
```

- But not if atomic loads are repurposed!!!

```
r2 =rlx x;
do_something(r2); // No synchronization or stores to x
int r0 =rlx x;
int r1 = r0 * r0 + 2 * r2 + 1;
```

No Atomic-Load Repurposing

- Guaranteed p re for small X:

```
r2 =r1
do_ ing(r2); // N chronization or stores to x
i 0 x;
i r1 = r 0 + 2 * r0 ;
```

- But if atomic lo re repurp d!!!

```
r rlx x;
do_ ething(r2); / chronization or stores to x
int lx x;
int r1 r2 + 1;
```

Instead, Merge the Atomic Loads

- Guaranteed perfect square for small X:

```
r2 =rlx x;
do_something(r2); // No synchronization or stores to x
int r0 =rlx x;
int r1 = r0 * r0 + 2 * r0 + 1;
```

- And that guarantee is maintained for merged loads:

```
r0 =rlx x;
do_something(r0); // No synchronization or stores to x
int r1 = r0 * r0 + 2 * r0 + 1;
```

Instead, Merge the Atomic Loads

- Guaranteed perfect square for small X:

```
r2 =rlx x;
do_something(r2); // No synchronizati                          to x
int r0 =rlx x;
int r1 = r0 * r0 + 2 * r0
```

- And that guarantee is n   ged loads:

```
r0 =rlx x;
do_so                   No synchronization or stores to x
                 r0 + 2 * r0 + 1;
```

If do_something() contains synchronization, then must keep both atomic loads

Atomic Loads and Memory Ordering

```
r1 =rlx X;                    X =rlx 1;
r2 =rlx Y;
Z =rlx (r1 == r2);
```

sdep?

Note: X, Y, and Z boolean and initially zero

See Section 4 (“C++ Compilers”)of P3692R2

Atomic Loads and Memory Ordering

```
r1a =rlx X;
r1b =rlx X; // Invented load
If (r1a != r1b) {
    Z =rlx 1;
    r2 =rlx Y;
} else {
    r2 =rlx Y;
    Z =rlx (r1b == r2);
}
```

~~sdep!~~

```
X =rlx 1;
```

Note: X, Y, and Z boolean and initially zero

Inventing atomic load likely also invents hundreds-of-cycles cache miss!!!

Atomic Loads and Memory Ordering

```
r1a =rlx X;
r1b =rlx X; // In      load
If (r1a != r1b
    Z =rlx 1
    r2 =rlx
} else {
    r2 =rlx Y
    Z =rlx (r1b    r2);
}
```

~~sdep!~~

```
X =rlx 1;
```

Note: X, Y, and Z boolean and initially zero

See Section 4.3 (“Inventing Atomic Loads Can Cause Errors and Destroy Semantic Dependencies”) of P3692R2

Non-Volatile Atomics Optimizations?

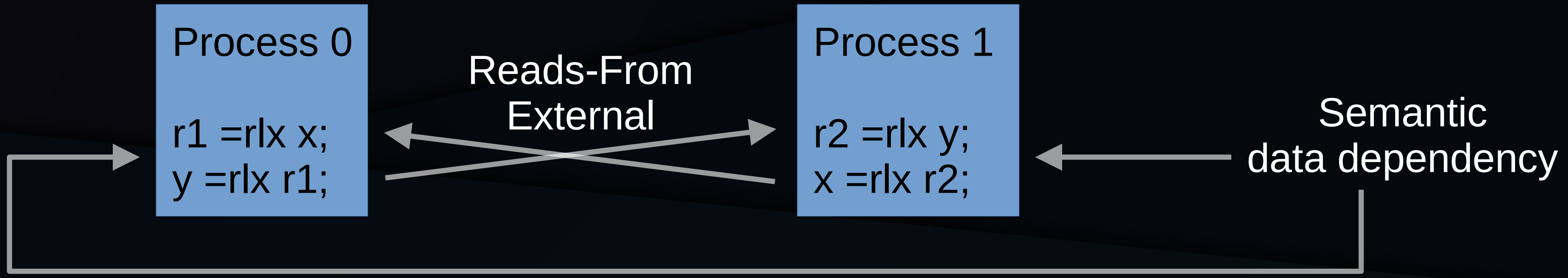
- Looking only at relaxed operations:
  - Reorder loads/stores from/to different objects
  - Merge back-to-back loads to same object
  - Drop loads whose values are unused
  - Discard first of back-to-back stores to same object
  - Fuse loads from (or stores to) adjacent objects if this results in a machine-word-sized/aligned access
  - But no invented, duplicated, or repurposed loads!!!

Tooling Looks at Object Code

See Section 7.3 (“Semantic Dependencies and Tooling”) and Appendix C (“But What About Tooling?”) of wg21.link/P3064R2

OOTA Cycles, Original Diagram

- Self-satisfying load-buffering cycle, x==y==42



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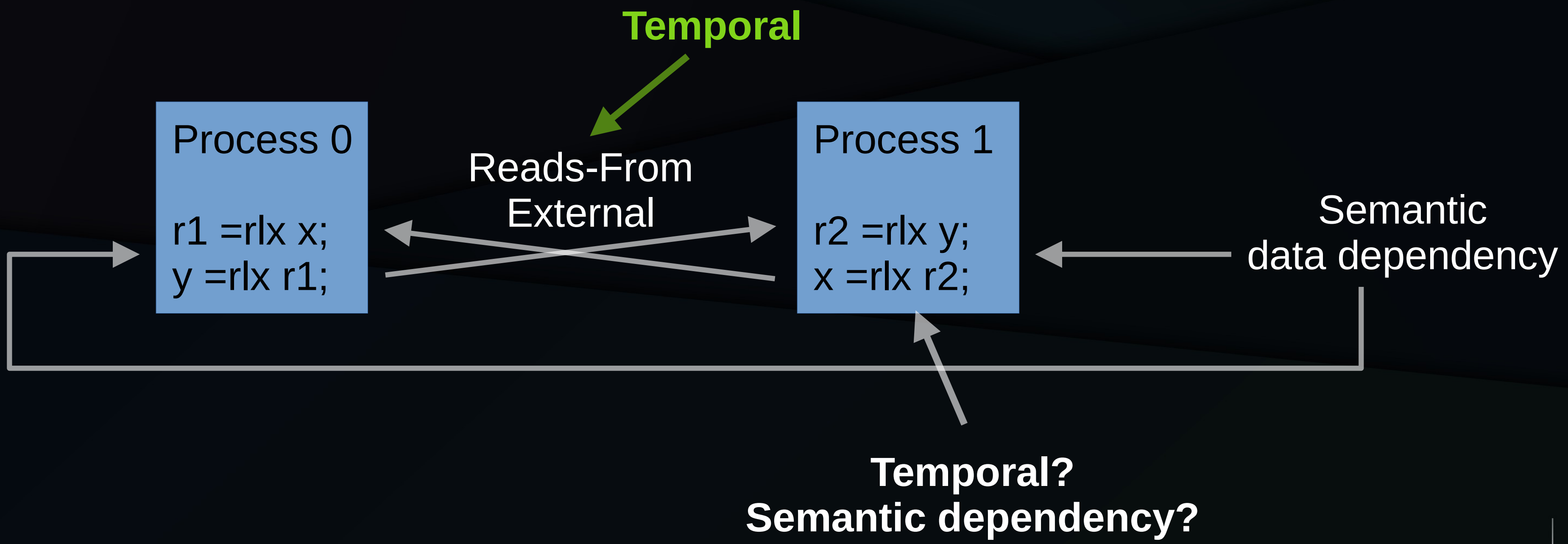
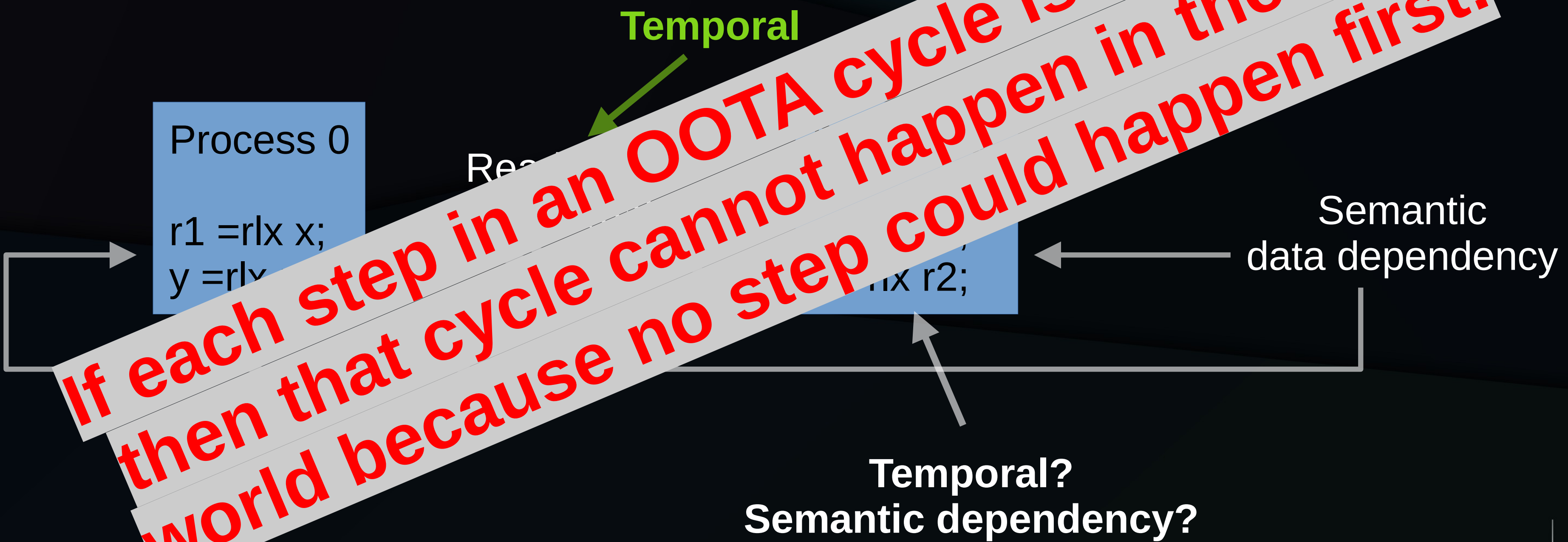


OOTA Cycles, Original Diagram

- Self-satisfying load-buffering cycl =42

If each step in an OOTA cycle is temporal, then that cycle cannot happen in the real world because no step could happen first!



Semantic Dependencies are Tricky

- At source-code level, semantic dependencies:
  - Are not strict functions of source code (Section 2.2.1)
  - Can be many-to-one (Section 2.2.2)
  - Depend on partially defined executions (Section 2.2.8-9)
  - Depend on compilers and their users (Section 2.2.8 & 4.1)
- Current paper assumes local analysis (no global cross-thread optimizations)

Semantic Dependencies in Code?

- Semantic dependencies are temporal:
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- Semantic dependencies are temporal:
  - Instructions take time to execute
  - Speculation must be checked against actual load
- Compiler optimizations break dependencies:
  - But HW memory models respect dependencies
  - Thus look at object code (seL4 verification approach)
  - Also look at other compiler-produced artifacts

See Sections 4-6, P3692R2

Semantic Dependencies in Code?

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  - Th (seL4 verification approach)
  - compiler-produced artifacts

If compiler optimizes dependency away, it was not semantic. Otherwise, executing dependency's code will take time.

Where Are We on OOTA? (Reprise)

- Generalized “OOTA Cycle” (Section 2.2.2)
- Fundamental property of semantic dependency (Sections 5.3 and 6.1)
- Demonstrate OOTA-freedom under restrictions (Sections 6.2 and 6.3 for demonstration, 4.4 for restrictions)
  - The main restriction is: No invented, duplicated, or repurposed atomic loads

Future Directions

- From compilers to (some) JITs, interpreters, and link-time optimizations (LTO)
- Compilers doing (some) global analysis given volatile atomics
- Identify absolute semantic dependencies inherent in source code
- Non-shared-memory communication

Discussion